REMARKS

Claims 1-10 and 24-26 are pending in the present application. Claims 11-23 are canceled herein without prejudice responsive to an election. Applicant notes that no new matter has been introduced as a result of the amendments presented herein.

Restriction

In the Office Action mailed January 26, 2005, in the above captioned case, the Examiner has stated that the present Application contains two distinct inventions. As such, the Examiner has required the Applicants to elect a single invention for prosecution on the merits. Specifically, the Examiner has required the Applicants to elect between a first invention, Group I, recited in Claims 1-10 and 24-26, drawn to a semiconductor device, classified in class 257, subclass 327, and a second invention, Group II, recited in Claims 11-23, drawn to method of making semiconductor devices, classified in class 438, subclass 212.

ELECTION WITHOUT TRAVERSE BETWEEN GROUP I AND GROUP II

Applicants elect without traverse Group I, recited in Claims 1-10 and 24-26, drawn to a semiconductor device, classified in class 257, subclass 327.

35 USC § 112

Claims 2 and 25 stand rejection under 35 USC § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Specifically, the rejection alleges that the specification does not refer to "a low gate-to-drain-capacitance on resistance product."

Applicants respectfully traverse. The present application teaches "the second portion of the gate region 320 and gate insulator region 325 acts to reduce the gate-to-drain capacitance (Cgd) of the device 300" (Figure 3, page 15 lines 4-5, *inter alia*). In addition, the present application teaches "the on resistance (Rds-on) of the device 300 is substantially equal to the legacy closed cell TMOSFET 200" (page 14 lines 19-20).

Applicants respectfully assert that these passages, among others, enable embodiments of the present invention as recited in Claims 2 and 25. Applicants respectfully assert that Claims 2 and 25 fully comply with 35 USC § 112, first paragraph, and consequently overcome the rejections of record. Applicants respectfully solicit allowance of these Claims.

35 USC § 102

Claims 1-6, 8-10 and 24-26 stand rejected under 35 USC § 102 as allegedly anticipated by Saito et al (US 2004/0165618, "Saito"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments of the present invention as recited in Claims 1-6, 8-10 and 24-26 are not anticipated or rendered obvious by Saito.

Applicant respectfully asserts that Saito does not teach or suggest the limitation of "a second portion of said drain region is separated from said normal-to-parallel structure" as recited by Claim 1. In contrast, Saito shows all drain regions overlapping the parallel structure. "Each gate electrode 24a has substantially a constant depth, and is formed to have a larger depth than that of the bottom of each p-type base layer 12a" [0047, emphasis added]. Further, Saito is silent as to a drain region separated from such a parallel or normal-to-parallel structure.

For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 2-10 depend from Independent Claim 1. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicit allowance of these Claims.

With respect to Claim 24, Applicant respectfully asserts that Saito does not teach or suggest the limitation of "a plurality of open gate-drain regions

arranged in a first plurality of parallel regions" as recited by Claim 1. Applicants respectfully assert that Saito is silent as to open gate-drain regions.

For this reason, Applicants respectfully assert that Claim 24 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 24, the rejection argues that an open gate-drain region is taught by Saito gate 24a-2. The gate-drain interface of gate 24a-2 differs from that of gate 24a-1 by gate-underlying p-type layers 14B. Saito further teaches, "[e]ach p-type layer 14B is formed to have impurity concentration lower than that of the p-type base layer 12a" [0048]. Saito is silent as to such concentration forming the recited "open gate-drain regions."

For this additional reason, Applicants respectfully assert that Claim 24 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 25-26 depend from Independent Claim 24. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicit allowance of these Claims.

35 USC § 103

Claim 7 stands rejected under 35 USC § 103 as allegedly anticipated by Saito et al (US 2004/0165618, "Saito") and further in view of Darwish et al. (US 2003/0062570, "Darwish"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claim 7 are not rendered obvious by Saito in view of Darwish.

Claim 7 depends from Independent Claim 1. Applicants respectfully assert that this Claim overcomes the rejections of record as it depends from an allowable base claim, and respectfully solicit allowance of this Claim.

CONCLUSION

Claims 1-10 and 24-26 are pending in the present application. Claims 11-23 are canceled herein responsive to an election. Applicant notes that no new matter has been introduced as a result of the amendments presented herein.

Applicants have reviewed the following references that were cited but not relied upon and do not find these references to teach or suggest the present claimed invention: US 6,627,950, US 2003/0178673, US 5,866,931, US 2001/0003367.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Date: 4/25/2005

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